FIG. 1

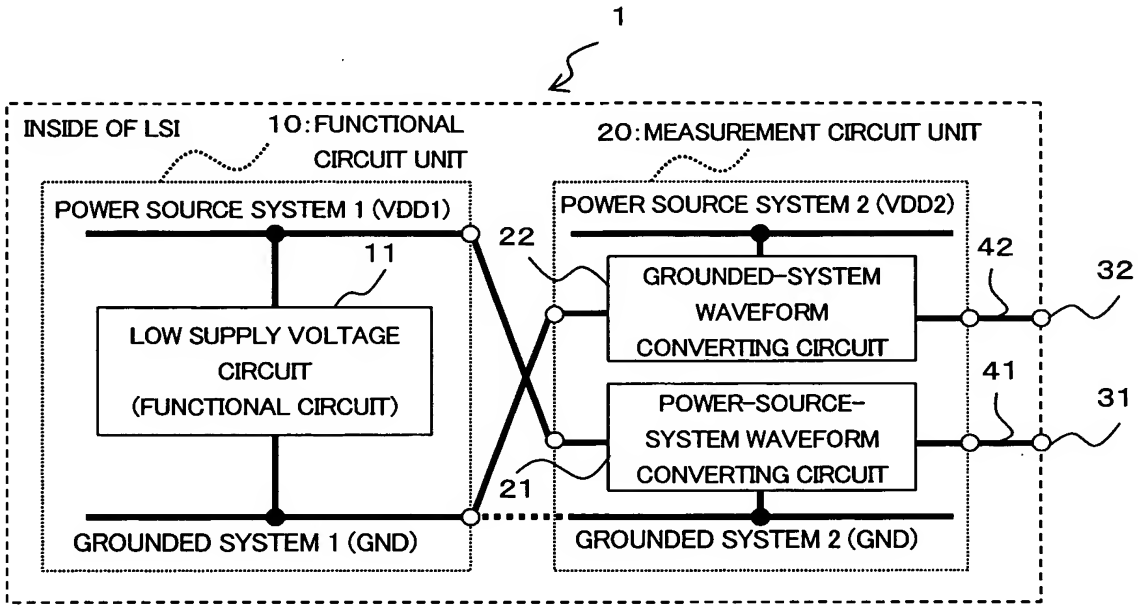


FIG. 2

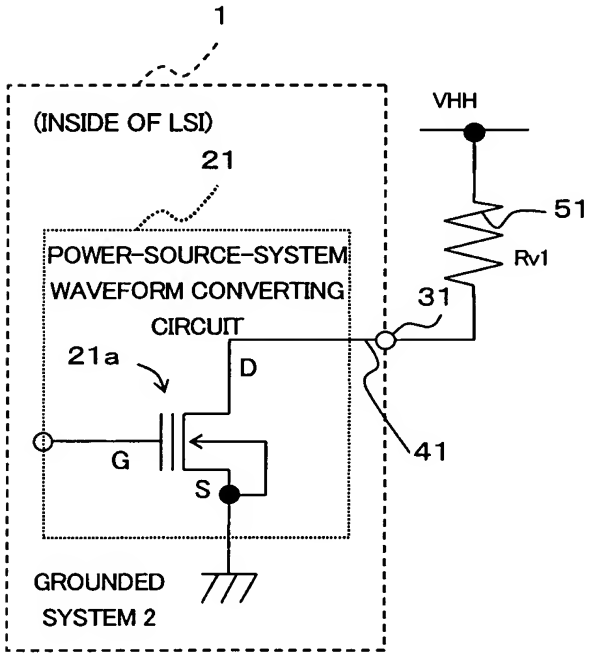


FIG. 3

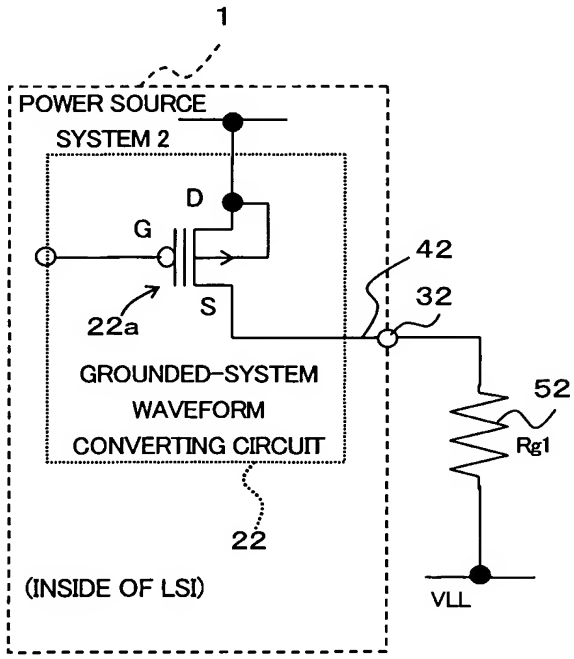


FIG. 4

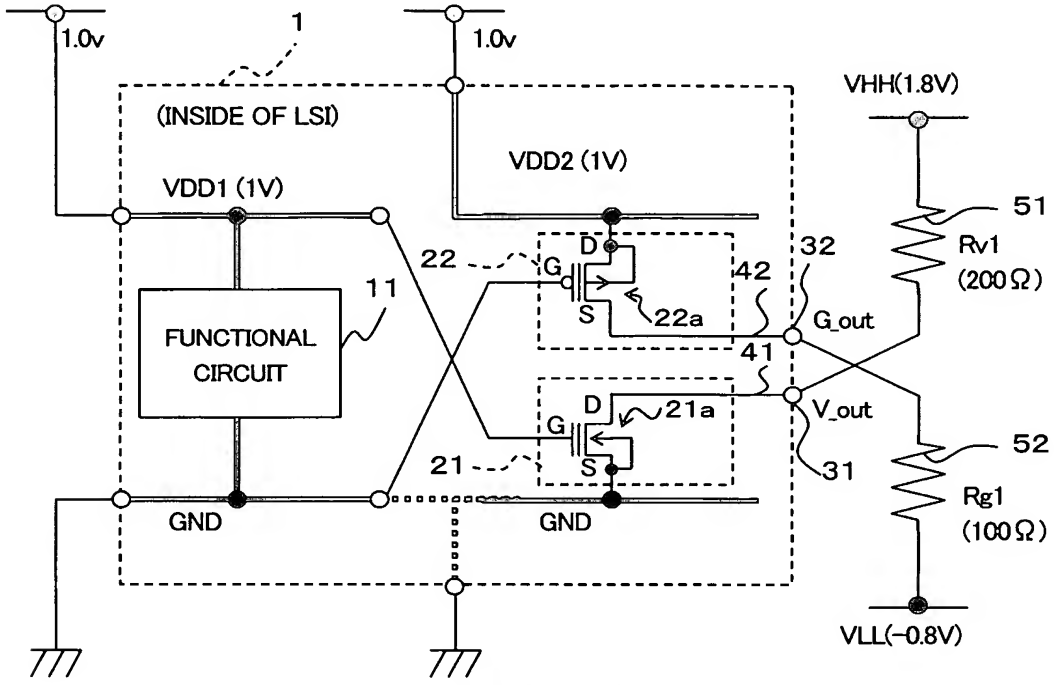

1.0v
1
1.0v
(INSIDE OF LSI)
VDD1 (1V)
VDD2 (1V)
VHH(1.8V)
51
Rv1
(200Ω)
22
D
G
S
22a
42
32
G_out
41
11
FUNCTIONAL
CIRCUIT
D
21a
G
V_out
S
21
31
52
Rg1
(100Ω)
GND
GND
VLL(−0.8V)

FIG. 5

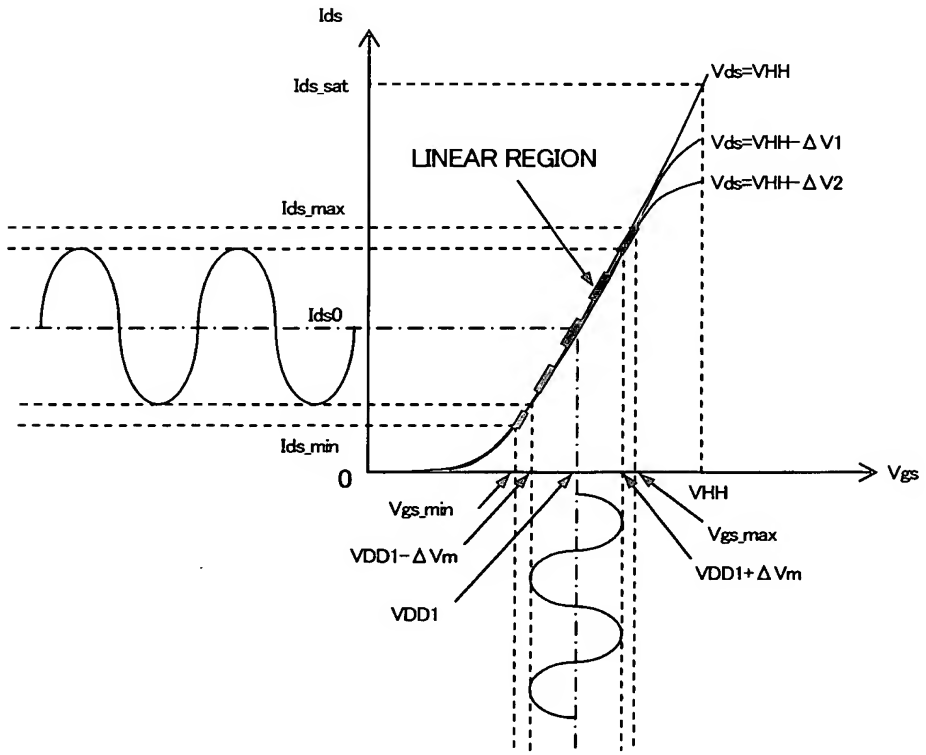

Ids
Ids_sat
Vds=VHH
Vds=VHH−ΔV1
LINEAR REGION
Vds=VHH−ΔV2
Ids_max
Ids0
Ids_min
0
Vgs
Vgs_min
VHH
Vgs_max
VDD1−ΔVm
VDD1+ΔVm
VDD1

FIG. 6

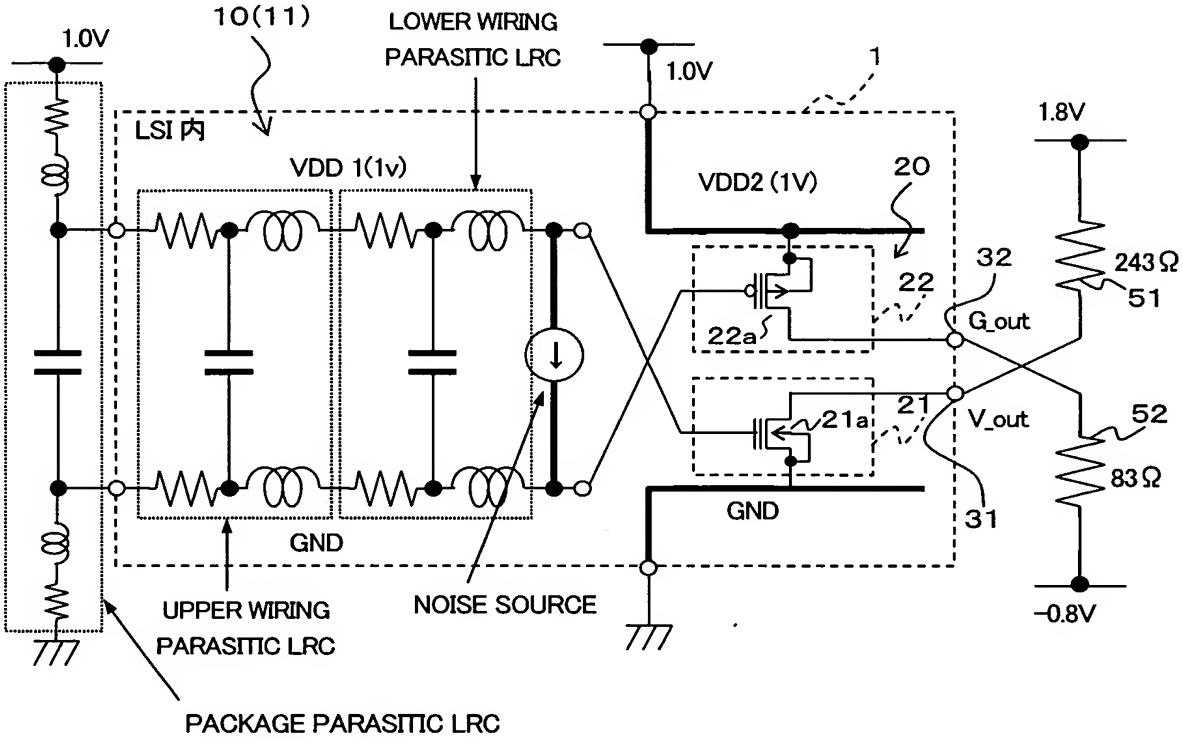

1.0V
10(11)
LOWER WIRING
PARASITIC LRC
1.0V
1
1.8V
LSI 内
VDD 1(1v)
VDD2 (1V)
20
32
243Ω
22
51
22a
G_out
21
21a
V_out
52
83Ω
GND
31
GND
UPPER WIRING
PARASITIC LRC
NOISE SOURCE
-0.8V
PACKAGE PARASITIC LRC

FIG. 7

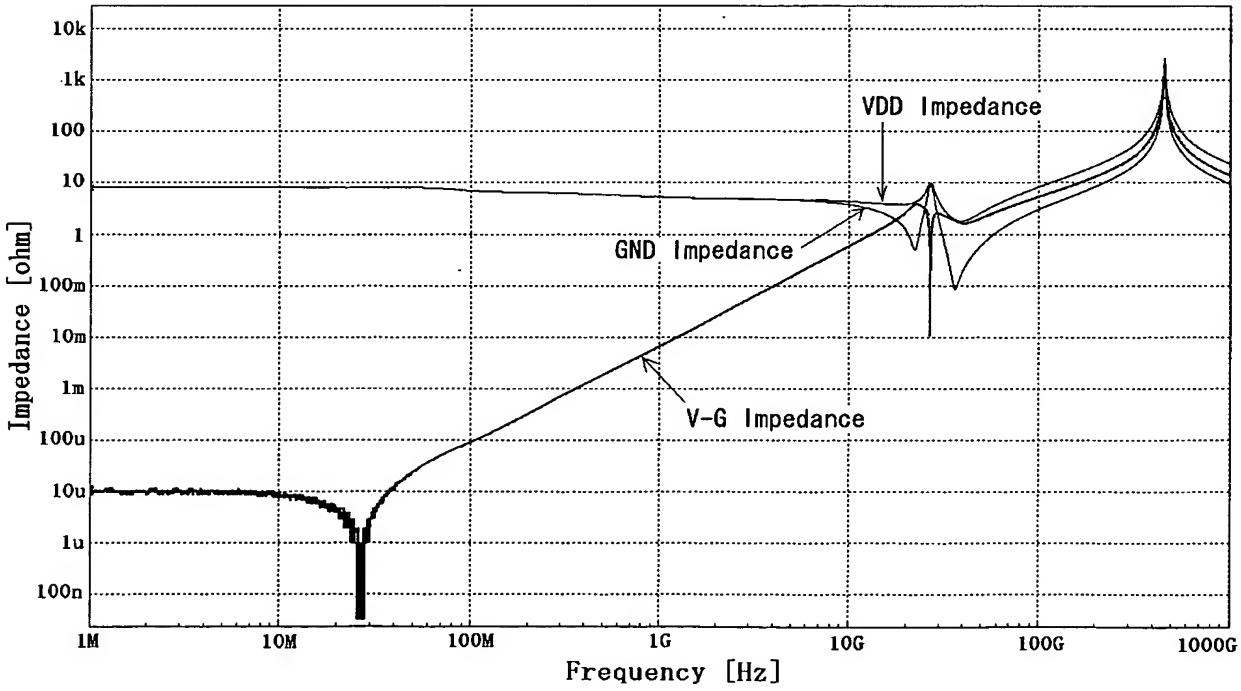

10k
1k
100
10
1
100m
10m
1m
100u
10u
1u
100n
Impedance [ohm]
VDD Impedance
GND Impedance
V-G Impedance
1M
10M
100M
1G
10G
100G
1000G
Frequency [Hz]

FIG. 8

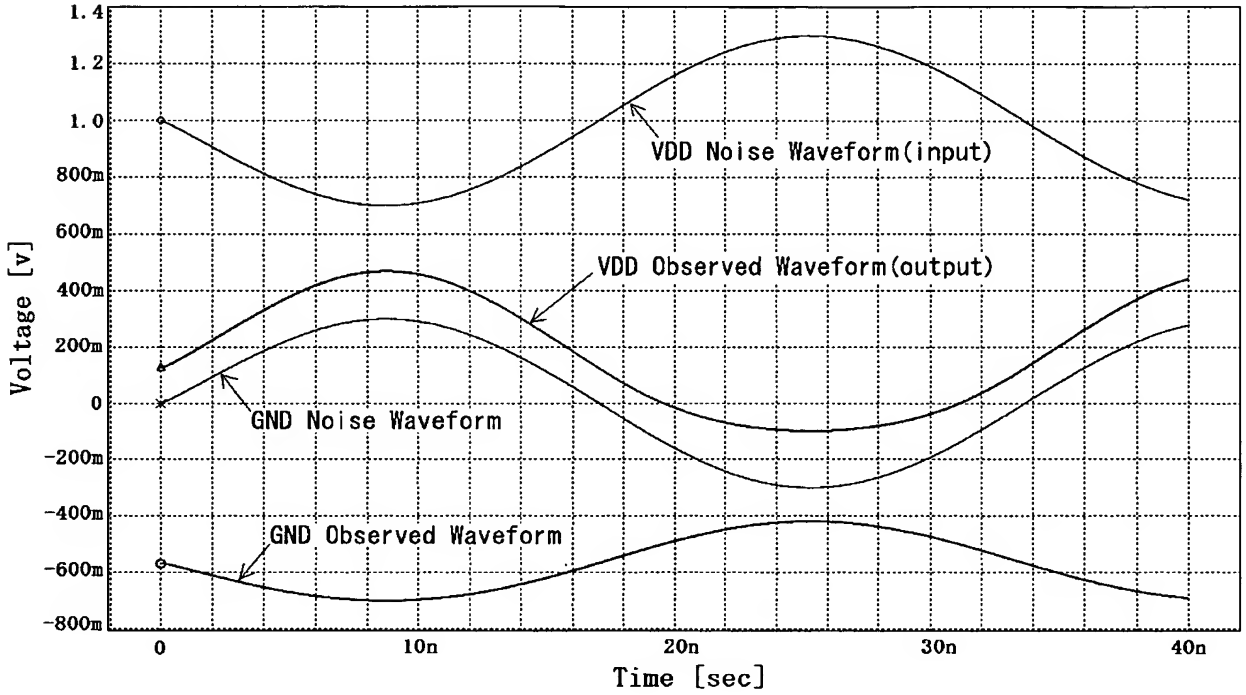

1.4
1.2
1.0
800m
600m
400m
200m
0
-200m
-400m
-600m
-800m
Voltage [v]
VDD Noise Waveform(input)
VDD Observed Waveform(output)
GND Noise Waveform
GND Observed Waveform
0
10n
20n
30n
40n
Time [sec]

FIG. 9

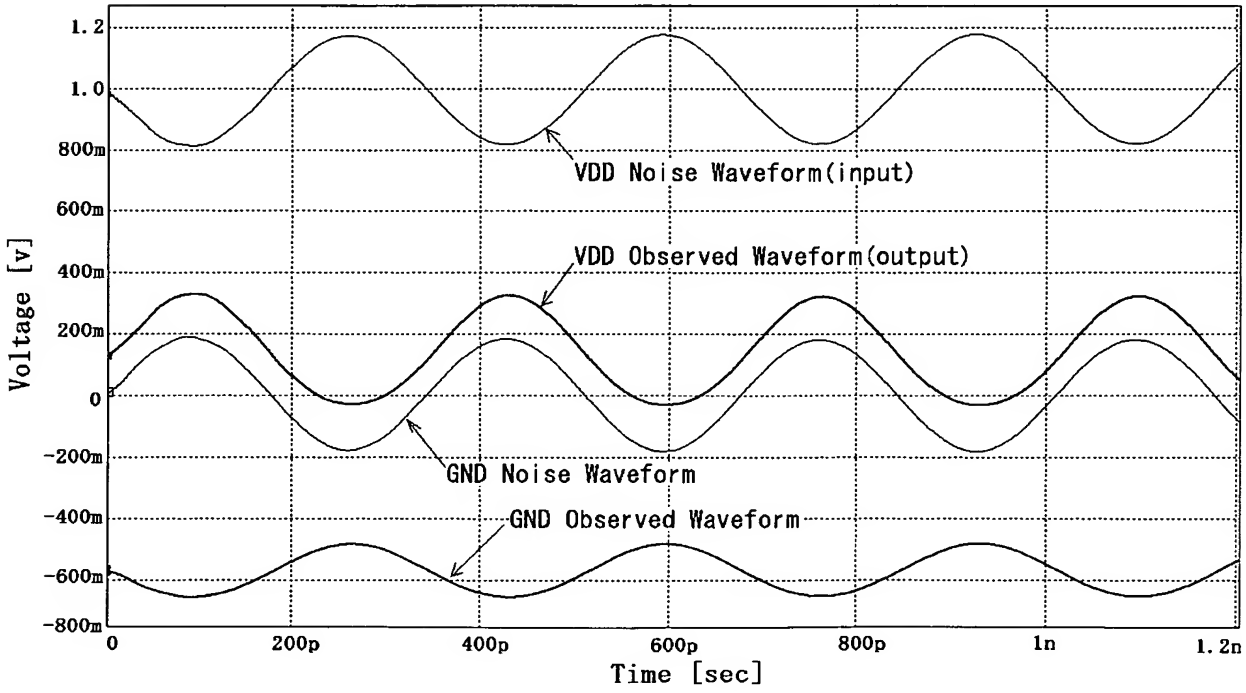

1.2
1.0
800m
600m
400m
200m
0
-200m
-400m
-600m
-800m
Voltage [v]
VDD Noise Waveform(input)
VDD Observed Waveform(output)
GND Noise Waveform
GND Observed Waveform
0
200p
400p
600p
800p
1n
1.2n
Time [sec]

FIG. 10

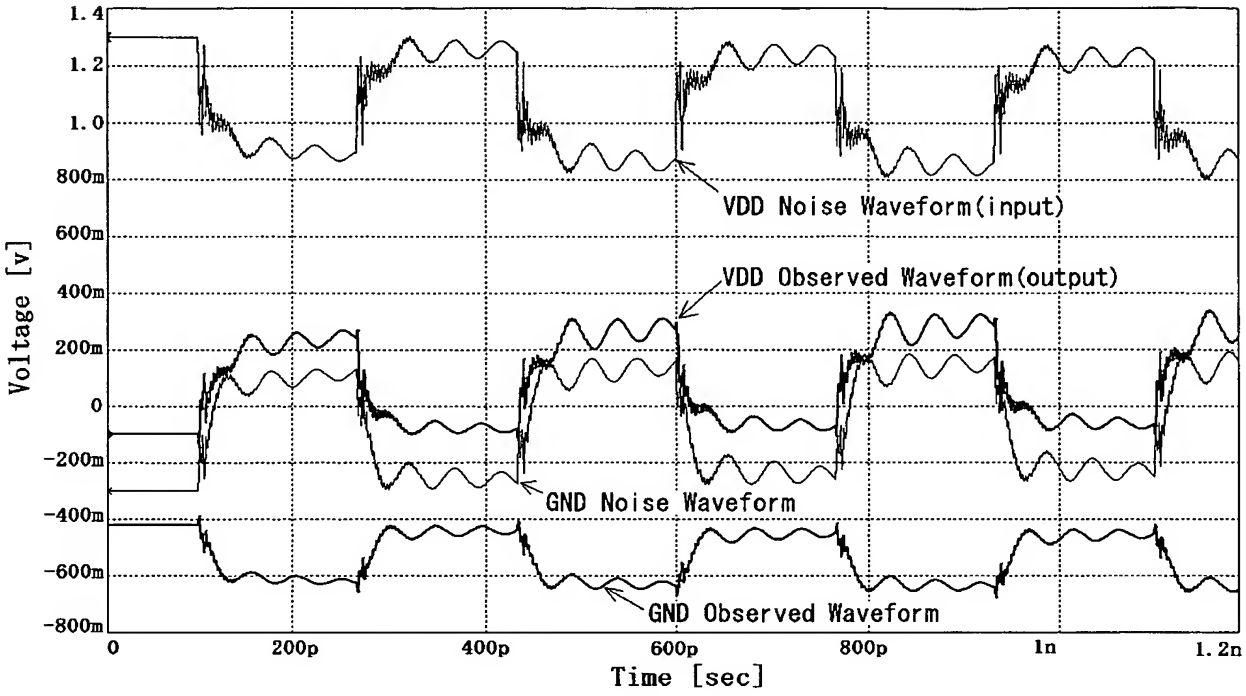

1.4
1.2
1.0
800m
600m
400m
200m
0
-200m
-400m
-600m
-800m
Voltage [v]
VDD Noise Waveform(input)
VDD Observed Waveform(output)
GND Noise Waveform
GND Observed Waveform
0
200p
400p
600p
800p
1n
1.2n
Time [sec]

FIG. 11

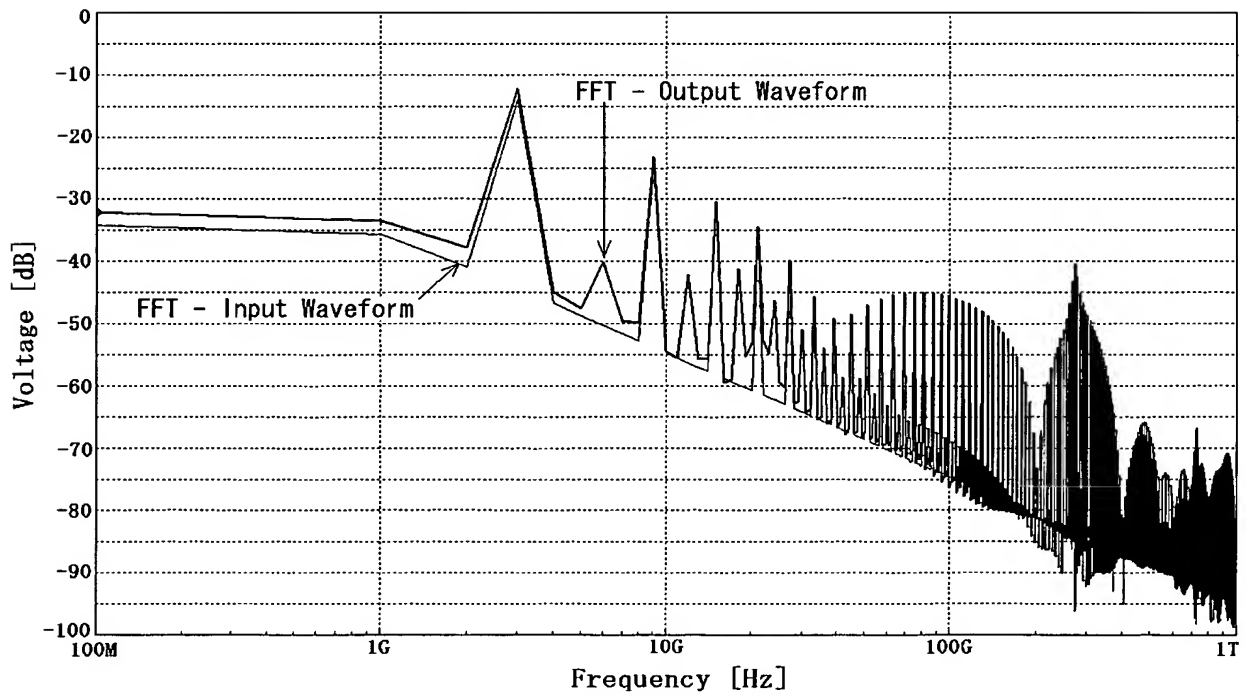

0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
Voltage [dB]
FFT - Output Waveform
FFT - Input Waveform
100M
1G
10G
100G
1T
Frequency [Hz]

FIG. 12

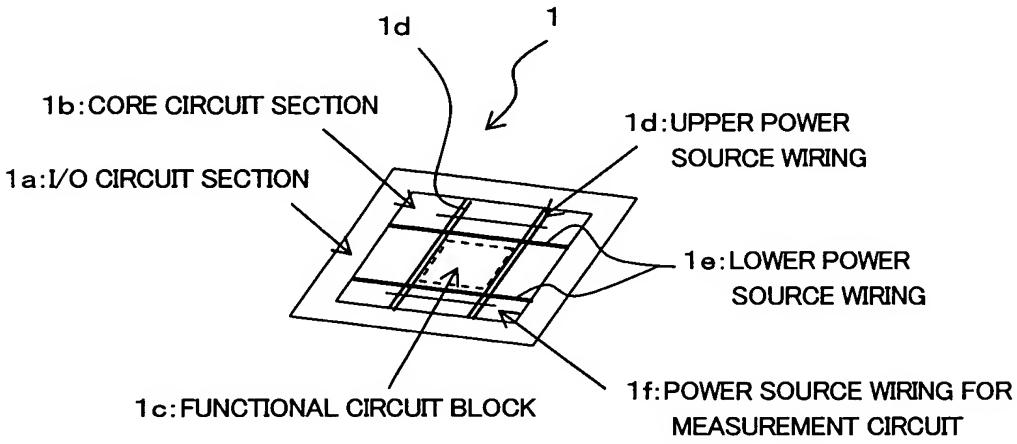

1d
1
1b:CORE CIRCUIT SECTION
1d:UPPER POWER SOURCE WIRING
1a:I/O CIRCUIT SECTION
1e:LOWER POWER SOURCE WIRING
1c:FUNCTIONAL CIRCUIT BLOCK
1f:POWER SOURCE WIRING FOR MEASUREMENT CIRCUIT

FIG. 13

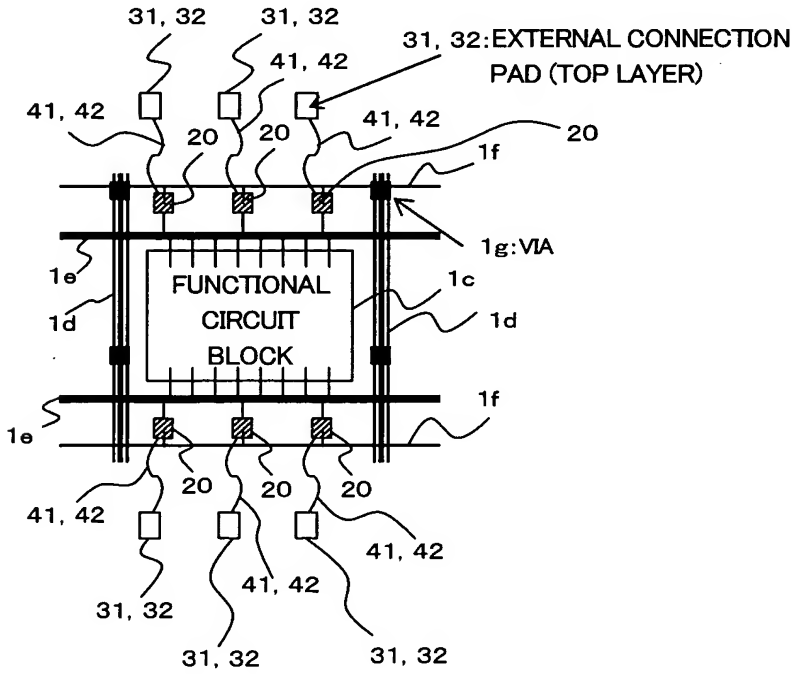

31, 32
31, 32
31, 32:EXTERNAL CONNECTION PAD (TOP LAYER)
41, 42
41, 42
41, 42
20
20
20
1f
1g:VIA
1e
1d
FUNCTIONAL CIRCUIT BLOCK
1c
1d
1f
1e
20
20
20
41, 42
41, 42
41, 42
31, 32
31, 32
31, 32

FIG. 14

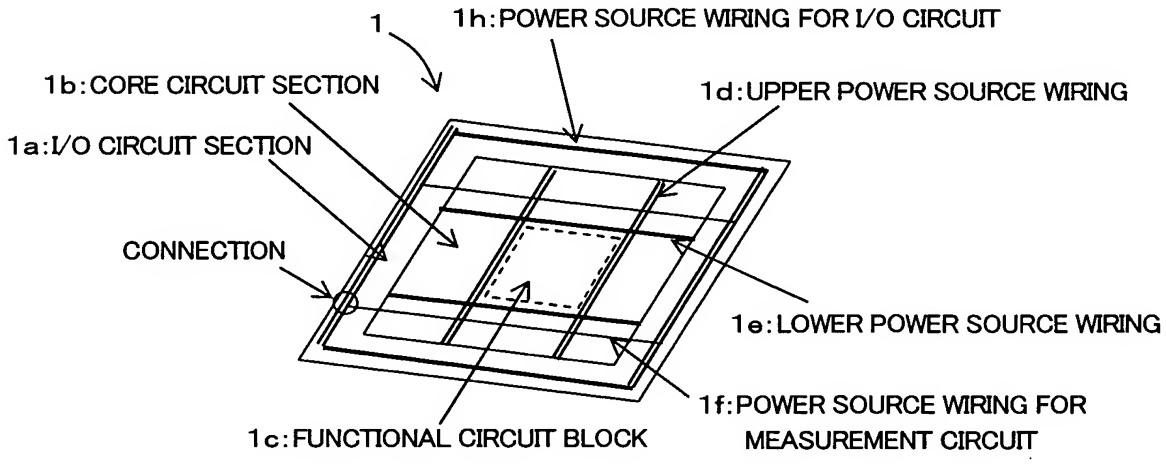

1
1h:POWER SOURCE WIRING FOR I/O CIRCUIT
1b:CORE CIRCUIT SECTION
1d:UPPER POWER SOURCE WIRING
1a:I/O CIRCUIT SECTION
CONNECTION
1e:LOWER POWER SOURCE WIRING
1f:POWER SOURCE WIRING FOR MEASUREMENT CIRCUIT
1c:FUNCTIONAL CIRCUIT BLOCK

FIG. 15

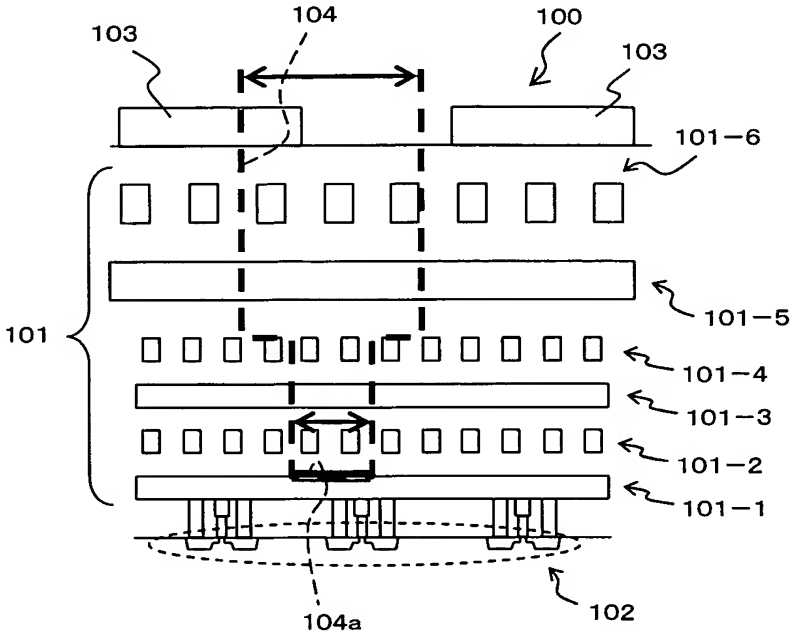
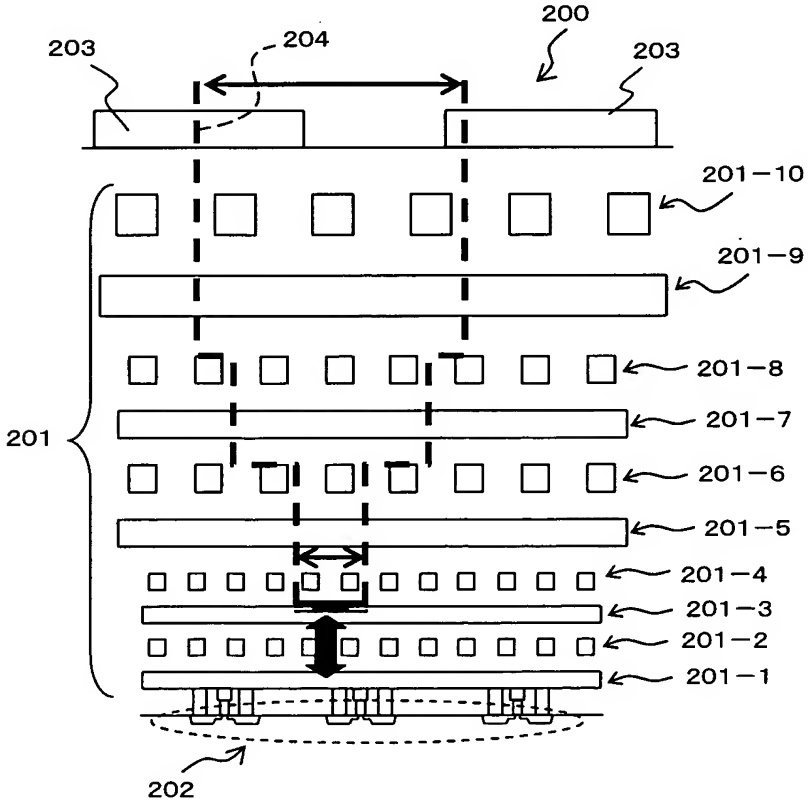

103
104
100
103
101-6
101
101-5
101-4
101-3
101-2
101-1
104a
102

FIG. 16


203
204
200
203
201-10
201-9
201-8
201
201-7
201-6
201-5
201-4
201-3
201-2
201-1
202